REMARKS

Summary of Office Action

Claims 1-37 were pending in the above-identified patent application.

Claim 5 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1—3, 5-10, 16-19, and 21-26 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lee et al. U.S. Patent No. 6,266,799 (hereinafter "Lee").

Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Li et al. U.S. Patent No. 6,693,985 (hereinafter "Li").

Claims 4, 20, and 27-37 were objected to as being dependent upon a rejected base claim.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of Applicants' Reply

Applicants have amended claim 5 to overcome the indefiniteness rejection. Applicants have also amended claim 25 to correct typographical errors and to more particularly define the claimed invention. No new matter has been added and the amendments are fully supported by the originally-filed specification.

The Examiner's rejections and objections are respectfully traversed.

Reply to the Rejection Under 35 U.S.C. § 112

Claim 5 was rejected under 35 U.S.C. § 112, second paragraph, because "the limitation of 'eighth circuitry' in line 3 as recited, is indefinite since - seventh circuitry --, has not been introduced previously" (Office Action, p. 2, ¶ 2). This rejection is respectfully traversed.

Applicants have amended claim 5 to properly recite "seventh circuitry" instead of --eighth circuitry--. Accordingly, applicants respectfully request the rejection to claim 5 be withdrawn.

Reply to the Objections and Rejections Under 35 U.S.C. §§ 102(e) and 103(a)

Claims 1–3, 5-10, 16-19, and 21-26 were rejected under 35 U.S.C. § 102(e) as being anticipated by Lee. Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Li. Claims 4, 20, and 27-37 were objected to as being dependent upon a rejected base claim. These rejections and objections are respectfully traversed.

Claims 1-24

Applicants' invention, as defined by independent claims 1 and 16, is directed to circuitry and a method for extracting data from a data signal having a data rate that is twice the frequency of a reference clock signal. A first phase-shifted version of the reference clock signal is derived that is synchronized with a rising edge (i.e., a 0-to-1 level transition) of the data signal. The data signal is sampled in a

predetermined phase relationship to this first phase-shifted version to extract a first partial stream of data. A second phase-shifted version of the reference clock signal is also derived that is synchronized with a falling edge (i.e., a 1-to-0 level transition) of the data signal. The data signal is further sampled in a predetermined phase relationship to this second phase-shifted version to extract a second partial stream of data.

Contrary to the Examiner's contentions, applicants respectfully submit that Lee does not show or suggest deriving first and second versions of the reference clock signal "that are respectively synchronized with oppositely polarized transitions in level of the data signal" as recited in applicants' independent claims 1 and 16.

Lee describes "methods and apparatus for implementing data/clock recovery systems in networking circuitry" (Lee, col. 1, lines 16-20). As shown and described in connection with FIGS. 2 and 3 of Lee, a multi-phase clock generator 204 generates multiple clock phases that are sent as input to a multi-phase data/clock recover unit 110(a). Unit 110(a) selects four of the clock phases (Φ_0, Φ_1, Φ_2, and Φ_3), samples the incoming data using the selected clock phases, determines whether the clock is leading or lagging the incoming data, and accordingly adjusts the clock by selecting another set of four clock phases. The data output from unit 110(a) is based on recovered clock phases Φ_0 and Φ_3. (Lee, FIGS. 2 and 3; and col. 5, line 23 to col. 6, line 43).

As shown and described in connection with FIG. 5 of Lee, the clock phase Φ_0 is mapped to the center of a first bit (data 0), the clock phase Φ_3 is mapped to the center of a second bit (data 1), the clock phase Φ_1 is mapped to a location just before a data transition from the first bit to the second bit (i.e., a rising edge), and the clock phase Φ_2 is mapped to a location just after the same data transition. All four clock phases are used to determine whether the clock phases are synchronized with the incoming data. (Lee, col. 7, lines 9-42).

In Lee, the four clock phases are respectively synchronized to the centers of each data bit, to a location just before a rising edge, and to a location just after a rising edge of the incoming data. Lee does not show or suggest one clock phase being synchronized with a rising edge and another clock phase being synchronized with a falling edge of the incoming data (i.e., "synchronized with oppositely polarized transitions in level of the data signal") as recited in applicants' independent claims 1 and 16.

For at least the foregoing reasons, applicants respectfully submit that independent claims 1 and 16 are allowable. Claims 2-15 and 17-24, which depend from independent claims 1 and 16, respectively, are therefore also allowable.

Claims 25-37

Applicants' invention, as defined by independent claim 25, is directed to an apparatus for receiving an information signal that includes data information and clock information for the data

information embedded in the information signal. The apparatus includes first input circuitry to receive the information signal and second input circuitry to receive a reference clock signal. Reference clock signal processing circuitry produces two recovered clock signals based on the information signal and the reference clock signal. Data recovery circuitry produces two retimed data output signals indicative of the data information in the information signal based on the information signal and the two recovered clock signals.

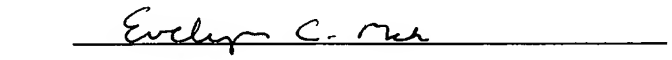
Applicants have amended independent claim 25 to more particularly define that the two recovered clock signals are each "respectively synchronized with oppositely polarized transitions in level of the information signal."

For at least the reasons given above with respect to independent claims 1 and 16, applicants respectfully submit that independent claim 25 is also allowable. Claims 26-37, which depend from independent claim 25, are therefore also allowable.

Conclusion

Applicants respectfully submit that this application, including claims 1-37, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully Submitted,



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